Sertifikaat

REPUBLIEK VAN SUID-AFRIKA

Certificate

PATENTKANTOOR 4

DEPARTEMENT VAN HANDEL EN NYWERHEID

REPUBLIC OF SOUTH AFRICA

PATENT OFFICE

DEPARTMENT OF TRADE AND INDUSTRY

Hiermee word gesertifiseer dat
This is to certify that

31/8

1556

1) South African Patent Application No. **2000/0887** accompanied by a Provisional Specification was filed at the South African Patent Office on the **23 February 2000**, in the name of **Potchefstroom University for Christian Higher Education** in respect of an invention entitled: **"Drive circuit and method for mosfet"**.

2) The photocopy attached hereto is a true copy of the provisional specification and drawings filed with South African Patent Application No. **2000/0887**.

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

RIA in die Republiek van Suid-Afrika, hierdie 22nd dag van March 2000
in the Republic of South Africa, this day of

Registrateur van Patente
Registrar of Patents

D.M. KISCH INC. , Johannesburg

Form P.1

INKOMSTE 23. 2. 00

REPUBLIEK VAN SUID-AFRIKA

REPUBLIC OF SOUTH AFRICA
PATENTS ACT, 1978

APPLICATION FOR A PATENT AND ACKNOWLEDGEMENT OF RECEIPT
(Section 30 (1) - Regulation 22)
The grant of a patent is hereby requested by the undermentioned applicant on the basis of the present application filed in duplicate.

PATENT APPLICATION NO.			AGENT'S REFERENCE
21	01	20000887	P/00/78204

FULL NAME(S) OF APPLICANT(S)

71 POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN HIGHER EDUCATION

2000 -02- 23

REPUBLIC OF SOUTH AFRICA

ADDRESS(ES) OF APPLICANT(S)

1 Hofmann Street
Potchefstroom

TITLE OF INVENTION

54 DRIVE CIRCUIT AND METHOD FOR MOSFET

THE APPLICANT CLAIMS PRIORITY AS SET OUT ON THE ACCOMPANYING FORM P.2.
The earliest priority claimed is

THIS APPLICATION IS FOR A PATENT OF ADDITION TO PATENT APPLICATION NO.	21	01	
THIS APPLICATION IS A FRESH APPLICATION IN TERMS OF SECTION 37 AND BASED ON APPLICATION NO.	21	01	

THIS APPLICATION IS ACCOMPANIED BY :

X	1	A single copy of a provisional ~~xxxxxxxxxxxxxxxxxxxxxxxx~~ specification of 6 pages.
X	2	Drawings of 2 sheets.
	3	Publication particulars and abstract (Form P.8. in duplicate).
	4	A copy of Figure of the drawings for the abstract.
	5	An assignment of invention.
	6	Certified priority document(s) (State number).
	7	Translation of priority document(s).
	8	An assignment of priority rights.
	9	A copy of Form P.2 and specification of S.A. Patent Application No. 21 01
	10	A declaration and power of attorney on Form P.3.
	11	Request for ante-dating on Form P.4.
	12	Request for classification on Form P.9.
	13	

DATED THIS 23 rd **DAY OF** February 2000

Patent Attorney for the Applicant(s)

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COMMISSION RECEIVED

OFFICIAL DATE STAMP
2000 -02- 23

PATENT OFFICE
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D.M. KISCH INC. , Johannesburg

Patent Attorneys & Trademark Agents
Attorneys & Notaries

Form P.6

REPUBLIC OF SOUTH AFRICA

PATENTS ACT, 1978.

PROVISIONAL SPECIFICATION

(Section 30 (1) - Regulation 27)

PATENT APPLICATION NO.			LODGING DATE.		AGENT'S REFERENCE
21	01	20000887	22	23-02-2000	P/00/78204

FULL NAME(S) OF APPLICANT(S)	
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FULL NAME(S) OF INVENTOR(S)	
72	VISSER, Barend

TITLE OF INVENTION	
54	DRIVE CIRCUIT AND METHOD FOR MOSFET

INTRODUCTION AND BACKGROUND TO THE INVENTION

This invention relates to a circuit and method for improving the switching speed of Field Effect Transistors (FET's), more particularly power FET's.

Capacitance inherent in transistor junctions limits the speed at which a voltage within a circuit can switch, owing to finite driving impedance or current. It is generally accepted that reducing the source impedances and load capacitances and increasing the drive currents within a circuit will improve switching times. It is also well known that the Miller effect can dominate high frequency performance of an amplifier driven by moderately high source impedance.

Prior art indicates a number of methods of alleviating the Miller effect in high frequency transistor switching circuits each functioning to reduce source impedance or reduce feedback capacitance, or both. Aside from this, the use of a simple ground-based amplifier alone (if the driving impedance is low enough) and the use of tuned circuits at the input and output of an amplifier reduces the undesirable effects of interelectrode capacitances.

Even with such improvements a MOSFET such as an IRF740 MOSFET typically switches through 200 volts in approximately 27ns at a peak current of 10 ampheres.

OBJECT OF THE INVENTION

It is an object of the present invention to provide a circuit and method for improving the switching time of FET's.

SUMMARY OF THE INVENTION

According to the invention there is provided a switch circuit for a field effect transistor (FET), the circuit comprising:

- charge storage means;
- switching means connected between the charge storage means and a gate of the FET;
- the switching means being operative to deposit charge from the storage means onto the gate, thereby to improve the rise-time of a signal in a drain-source circuit of the FET.

With appropriate voltages at the gate, the switching means may also be operative to drain charge from the gate onto the charge storing means, thereby to improve the switching time of a signal in the drain-source circuit of the FET.

The switching means may comprise a SIDAC.

The charge storage means may comprise a capacitor.

The circuit may be built up from discrete components packaged in separate packages alternatively it may be packaged in one package. Further alternatively, the circuit may be integrated on a single chip.

Further according to the invention there is provided a method of operating a field effect transistor (FET) comprising the steps of applying charge of one polarity on a gate of the FET to drive it beyond a gate threshold voltage, before onset of conduction in a drain-source circuit of the FET.

Further according to the invention the method may also include the step of applying charge of an opposite polarity to the gate, to drive it below the gate threshold voltage, before conduction in the drain source circuit decreases.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described, by way of example only, with reference to the accompanying drawings wherein:

figure 1 is a schematic diagram of a circuit according to the invention; and

figures 2(a)(b) and (c) are graphical representations of current as applied to the gate; gate voltage changes resulting from the combined effect of gate current and the onset of drain-source switching; and the resulting drain-source current, respectively.

DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring to figure 1, a circuit according to the invention implementing a method according to the invention for decreasing the switching time of a power, field effect transistor is schematically illustrated and referenced 10.

A periodic voltage is applied across a capacitor 12, in parallel with a SIDAC 14 and a MOSFET 16, such as an IRF740. Initially, during a first half cycle, the voltage supplied at the input 17 is insufficient to switch the SIDAC 14 on and the capacitor 12 is hence charged up. When the supplied voltage reaches the threshold of the SIDAC 14 it switches on, resulting in a closed circuit from the capacitor 14 to the gate 18 of the MOSFET 16, partially discharging the capacitor 12 and hence charging the gate 18. The result is that a charge will now be shared between the capacitor 12 and the gate 18, so that some voltage, preferably above the gate threshold voltage relative to ground, is applied to the gate.

A time diagram of the resulting currents and voltages as measured at the gate 18 of the MOSFET 16 relative to ground potential is shown in figure 2. As shown in figure 2(a) the current that discharges from the capacitor 12 through the SIDAC 14 is applied to the gate 18 of the MOSFET 16 slightly prior to the onset of current flow I_d in the drain-source circuit 20

of the FET 16. As a result of the current from the capacitor, the voltage on the gate exceeds the threshold voltage 22 by a sufficient amount.

Using this method, the gate voltage may for short intervals be driven approximately three to four times beyond the maximum threshold rating of some MOSFET's 16 without destroying the device.

Similarly, when during the other half cycle the gate voltage exceeds the reverse threshold of the SIDAC 14 and current is conducted in the opposite direction, the gate voltage of the MOSFET 16 drops to below the threshold voltage of the MOSFET 16 shortly after the charge dissipates from the gate 18 of the MOSFET 16. As a result, the MOSFET 16 will turn off and the drain current will no longer flow.

It has been found that with the circuit of figure 1 a resulting voltage signal in the drain-source circuit of the FET switches on and off through 200V within about 3 to 5 ns.

It will be appreciated that a number of variations in detail on the circuit and method according to the invention are possible without departing from the scope and or spirit of this disclosure.

Dated this 23 day of February 2000

Patent Attorney / Agent for the Applicant

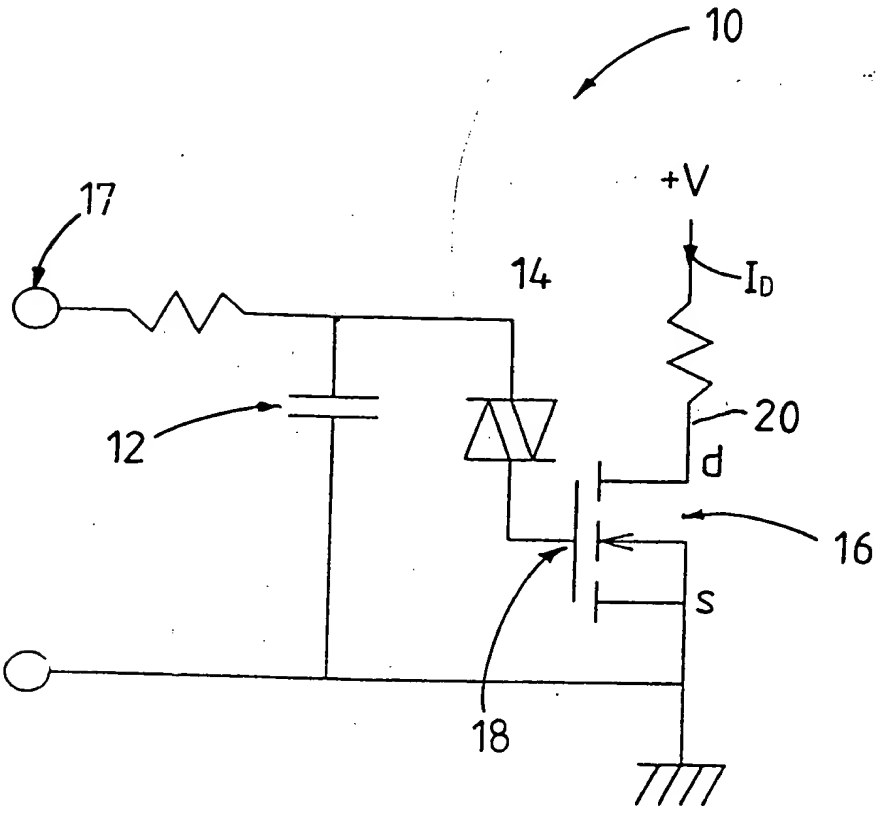

FIGURE 1

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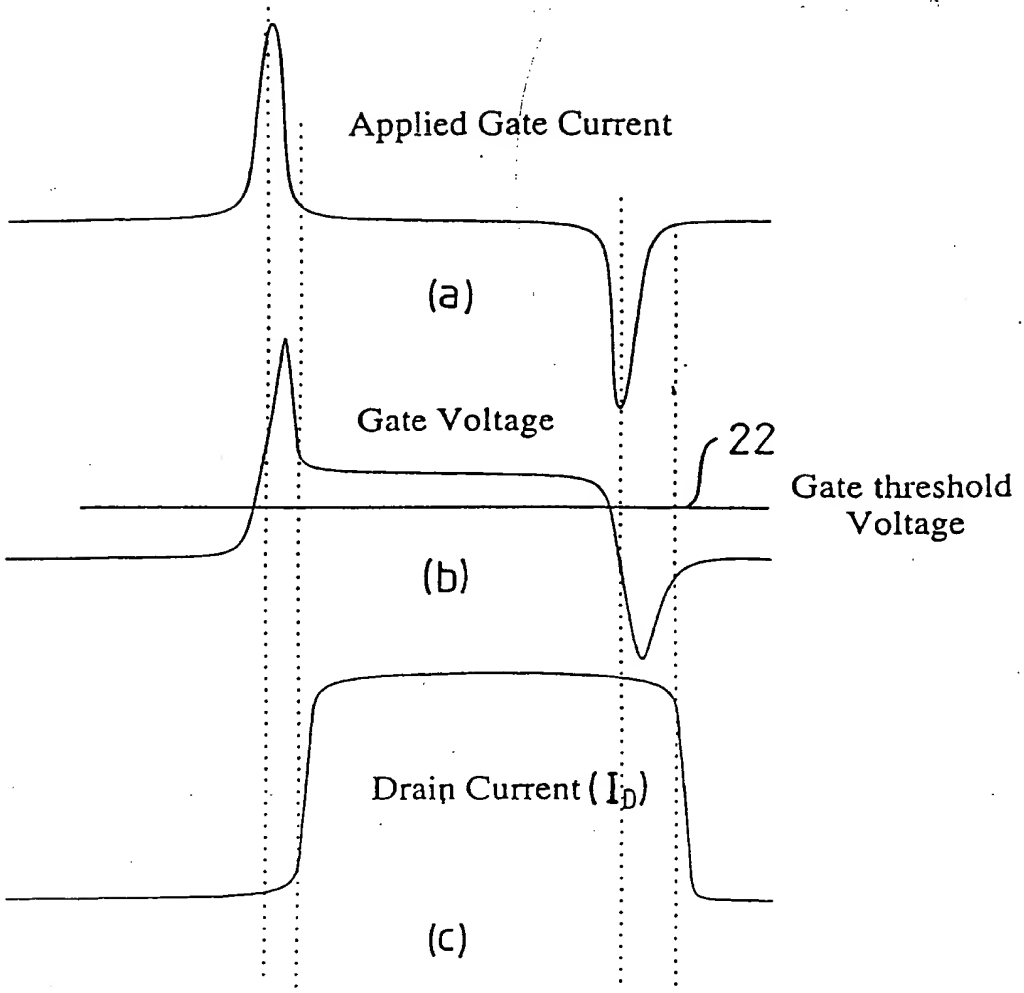

FIGURE 2

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